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EXAMINER
MOORE, WILLIAM P

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 12/27/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/598,210	NILSSON, JOHAN	
	Examiner	Art Unit	
	William P Moore	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 11-16* is/are rejected.

7)☒ Claim(s) *8,9,17 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06/21/00* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

Statement of Statutory Basis

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 5, 6

2. Claims 1, 2, 5, 6 are rejected under 35 U.S.C 102(b) as being anticipated by ABE et al. (EPO 0,600,095 A1).

Abe et al. discloses as per claim 1:

using an error correction decoding technique to generate a block of decoded bits from the received signal (See Figure 1 where, error correction decoding technique of block 20, generates a block of decoded bits on signal S20 from the received signal S21a. See Column 4, Lines 10-15.)

using an error detection technique to determine whether at least one of the decoded bits from the block of decoded bits has an erroneous value (See Figure 1, where error detection technique is shown as part of block 20 to determines whether at least one of the decoded bits from the block of decoded bits 21a has an erroneous value on signal S21b. See Column 4, lines 10-23 or more specifically

lines 15-23 that describe the error detection technique used in block 20 (this detection technique is used in combination with a viterbi error correction decoding technique lines 10-15*)* ABE et al. describes the error detection technique as detecting an overflow condition in the viterbi decoder and producing an overflow signal. Also, detection of this overflow condition in combination with exceeding an appropriately set threshold value, lines 20-23, is equivalent to determining whether at least one of the decoded bits has a non-correctable error or in other words one of the decoded bits from the block of decoded bits has an erroneous value.)

if none of the decoded bits from the block of decoded bits has an erroneous value, then calculating the bit error rate (BER) estimate from the received signal (See Figure 1, where the switch part 23, checks signal s22 that indicates if none of the decoded bits from the block of decoded buts has an erroneous value, then if this condition is true, the switch selects the bit error rate estimate from the received signal 23, which causes bit error rate estimate to be calculated from the received signal S20 and output on signal S25. See Column 3, Lines 10-39 or more specifically lines 23-26 which describes how the switch part 23 selects the decoded bits when no switch instruction is applied. This switch instruction is generated only when there are no non-correctable errors in the decoder 21, or in other words, none of the decoded bits from the block of decoded bits has an erroneous value.)

if at least one of the decoded bits from the block of decoded bits has an erroneous value, then setting the bit error rate (BER) estimate equal to a value that is based on a previously calculated bit error rate(BER). (See Figure 1, where the switch part 23, checks signal s22 that indicates the equivalent of at least one of the decoded bits from the block of decoded bits has an erroneous value, then if this condition is true, the switch selects a preset bit error rate(column 3, lines 53-56). Also, claims of Abe et al. are within the scope of a *previously calculated BER* since a *previously calculated BER* is a type of *preset BER* whether it is calculated and loaded statically during initialization or based dynamically on the state of the design. See claim 4, "set value output means for outputting the preset bit error rate".)

Abe et al. discloses as per claim 2:

using the error detection technique to generate error detection information from the block of decoded bits. (See Figure 1, where error detection technique is performed by block 20 to generate error detection information S21b and S22 from the block of decoded bits.)

processing the block of decoded bits and the error detection information to generate a synthesized block of coded bits wherein the processing includes using an error correction coding technique that corresponds to the error correction decoding technique (See Figure 1, the re-encoding part 24 processes the block of decoded bits on bus S21a and the error detection information on bus S22 to generate a synthesized block of coded bits S24 wherein the processing includes

using an error correction coding technique part of block 24 that corresponds to the error correction decoding technique part of block 21.)

using a non-error correction decoding technique to generate a block of raw decoded bits from the received signal. (Applicant defines raw decoding on Page 4, lines 25-26 as merely generating 1's and 0's from received signals. By definition this is equivalent to demodulating the signal prior to applying error correction decoding. Since Abe et al. discloses a digital communication system with error correction it must contain a demodulate the signal prior to applying error correction decoding.)

comparing each bit of the synthesized block of coded bits with a corresponding bit of the block of raw decoded bits (See Figure 1, Comparator Part 25 compares each bit of the synthesized block of coded bits S24 with a corresponding bit of the block of raw decoded bits S26.)

setting the bit error rate estimate equal to a value that represents how many bits of the synthesized block of coded bits are not equal to the corresponding bits of the block of raw decoded bit (See Figure 1, Comparator Part 25 outputs the bit error rate on bus S25.It old and well known in the art that bit error rate is defined as the number of errors during a given period. Thus, the bit error rate that is set on S25 is equal to a value that represents how many bits of the synthesized block of coded bits (S24) are not equal to the corresponding bits of the block of raw decoded bit S26.)

Abe et al. discloses as per claim 5:

the error detection technique includes calculating a cyclic redundancy check. (Claim 1, col. 27, lines 3-7, shows that the scope of their invention is applicable to any type of error correction decoding technique. Therefore, using cyclic redundancy check codes for error detection and correction fall with in the scope of the invention of Abe et al.)

Abe et al. discloses as per claim 6:

the error correction decoding technique includes using Viterbi processing. (See Column 4, lines 10-15 that discloses the use of viterbi for error correction decoding)

Claims 10, 11, 14, 15

3. Claims 10, 11, 14, & 15 are rejected under 35 U.S.C 102(b) as being anticipated by ABE et al. (EPO 0,600,095 A1).

Abe et al. discloses as per claim 10:

logic that uses an error correction decoding technique to generate a block of decoded bits from the received signal. (See Figure 1 that discloses logic that uses an error correction decoding technique of block 20 to generates a block of decoded bits on signal S20 from the received signal S21a. See Column 4, Lines 10-15.)

logic that uses an error detection technique to determine whether at least one of the decoded bits from the block of decoded bits has an erroneous value (See Figure 1, that discloses logic that uses an error detection technique shown as part of block 20 to determines whether at least one of the decoded bits from the

block of decoded bits 21a has an erroneous value on signal S21b. See Column 4, lines 10-23 or more specifically lines 15-23 that describe the error detection technique used in block 20 (this detection technique is used in combination with a viterbi error correction decoding technique lines 10-15*)* ABE et al. describes the error detection technique as detecting an overflow condition in the viterbi decoder and producing an overflow signal. Also, detection of this overflow condition in combination with exceeding an appropriately set threshold value, lines 20-23, is equivalent to determining whether at least one of the decoded bits has a non-correctable error or in other words one of the decoded bits from the block of decoded bits has an erroneous value.)

logic that calculates the bit error rate estimate from the received signal if none of the decoded bits from the block of decoded bits has an erroneous value (See Figure 1 that discloses logic (25, 24, 23, 22) that calculates the bit error rate estimate and output its value on signal S25 using comparison logic unit 25 if none of the decoded bits from the block of decoded bits output on S21a has an erroneous value flagged by signal S21b and S22. Logic of Switching unit 23 performs previously mentioned "if" comparison by comparing error flags from decoder. See Column 3, Lines 10-39 or more specifically lines 23-26 which describes how the switch part 23 selects the decoded bits when no switch instruction is applied. This switch instruction is generated only when there are no non-correctable errors in the decoder 21, or in other words, none of the decoded bits from the block of decoded bits has an erroneous value.)

logic that sets the bit error rate estimate equal to a value that is based on a previously calculated bit error rate if at least one of the decoded bits from the block of decoded bits has an erroneous value. (See Figure 1 that discloses logic that sets the bit error rate estimate equal on signal S23a to a value that is based on a preset calculated bit error rate (col. 4, ll. 27, "a set bit error rate". col. 3, ll. 53-56) if at least one of the decoded bits from the block of decoded bits has an erroneous value (col. 4, ll.15-28, exceeding the overflow threshold in the viterbi decoder is equivalent to checking if at least one of the decoded bits from the block of decoded buts has an erroneous value) The claimed logic is composed of switch part 23 that checks signal s22 which indicates the equivalent of at least one of the decoded bits from the block of decoded bits has an erroneous value, then if this condition is true, the switch selects a preset bit error rate(column 3, lines 53-56) or as is within the scope of a preset bit error rate, a previously calculated bit error rate. See Column 3, lines 53-56, and Column 4, Lines 23-28.)

Abe et al. discloses as per claim 10:

logic that uses the error detection technique to generate error detection information from the block of decoded bits (See Figure 1, where logic (20) that uses the error detection technique is performed by block 20 to generate error detection information S21b and S22 from the block of decoded bits.)

processing logic that processes the block of decoded bits and the error detection information to generate a synthesized block of coded bits, wherein the processing logic includes logic that uses an error correction coding technique that

corresponds to the error correction decoding technique (See Figure 1, processing logic (re-encoding part 24) that processes the block of decoded bits on bus S21a and the error detection information on bus S22 to generate a synthesized block of coded bits S24, wherein the processing logic (24) includes logic that uses an error correction coding technique part of block 24 that corresponds to the error correction decoding technique part of block 21.)

Logic that uses a non-error correction decoding technique to generate a block of raw decoded bits from the received signal (Applicant defines raw decoding on Page 4, lines 25-26 as merely generating 1's and 0's from received signals. By definition this is equivalent to demodulating the signal prior to applying error correction decoding. Since Abe et al. discloses a digital communication system with error correction it must inherently demodulate the signal prior to applying error correction decoding.)

logic that compares each bit of the synthesized block of coded bits with a corresponding bit of the block of raw decoded bits (See Figure 1, logic that compares (comparator 25), compares each bit of the synthesized block of coded bits S24 with a corresponding bit of the block of raw decoded bits S26.)

logic that sets the bit error rate estimate equal to a value that represents how many bits of the synthesized block of coded bits are not equal to the corresponding bits of the block of raw decoded bits. (See Figure 1, logic 25 sets the bit error rate estimate on bus S25. It is old and well known in the art that bit error rate is defined as the number of errors during a given period. Thus, the bit

error rate that is set on S25 is equal to a value that represents how many bits of the synthesized block of coded bits (S24) are not equal to the corresponding bits of the block of raw decoded bit S26.)

Abe et al. discloses as per claim 14:

the error detection technique includes calculating a cyclic redundancy check. (Claim 1, col. 27, lines 3-7, shows that the scope of their invention is applicable to any type of error correction decoding technique. Therefore, using cyclic redundancy check codes for error detection and correction fall with in the scope of the invention of Abe et al.)

as per claim 15:

the logic that uses the error correction decoding technique includes a Viterbi decoder. (See Column 4, lines 10-15 that discloses the use of viterbi for error correction decoding.)

Claim Rejections - 35 USC 103

Statement of Statutory Basis

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 3

5. Claim 3 (dependent on claim 1) is rejected under 35 U.S.C. 103(a) as being unpatentable over Abe et al. (EPO 0,600,095 A1)

Abe et al discloses all of the elements recited by claim 1. (see rejection of claim 1 under 35 USC 102(b))

Abe et al does not explicitly disclose the step of setting the bit error rate estimate equal to the value that is based on the previously calculated bit error rate comprises setting the bit error rate estimate equal to a value that is equal to the previously calculated bit error rate.

Abe et al Teaches in Column 3, lines 40-47 that the calculated BER is not accurate when an error occurs during decoding.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify Abe et al. such that it contains logic to disable updating the BER register that receives the calculated BER when an error occurs during decoding. (or equivalently, setting the bit error rate estimate equal to a value that is equal to the previously calculated bit error rate.) The effect of doing this would cause the previously calculated BER to be used as the current BER.

The motivation for making this modification would be to prevent updating the BER with an inaccurate BER calculation when an error occurs during decoding. (Column 3, lines 40-47)

Claim 4

6. Claim 4 (dependent on claim 1) is rejected under 35 U.S.C. 103(a) as being unpatentable over Abe et al. (EPO 0,600,095 A1).

Abe et al discloses all of the elements recited by claim 1. (see rejection of claim 1 under 35 USC 102(b))

Abe et al does not explicitly disclose the step of setting the bit error rate estimate equal to the value that is based on the previously calculated bit error rate comprises: setting the bit error rate estimate equal to a value that is predicted from one or more previously calculated bit error rates.

Abe et al Teaches in Column 3, lines 40-47 that the calculated BER is not accurate when an error occurs during decoding.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify Abe et al. such that it includes logic for averaging previously calculated BER in order to calculate a preset value for assignment as an estimated BER in the case where a decoder error has occurred.

The motivation for making this modification would be to prevent updating the BER with an inaccurate BER calculation when an error occurs during decoding.

Claim 7

7. Claim 7 (dependent on claim 1) is rejected under 35 U.S.C. 103(a) as being unpatentable over ABE et al.(EPO 0,600,095 A1) in view of Paik et al. (US Patent 5,241,563) in view of Wicker ("Error Control Systems for Digital Communication and Storage", Prentice-Hall, 1995).

Abe et al. discloses all of the elements recited by claim 1. (see rejection of claim 1 under 35 USC 102(b))

Abe et al. does not disclose:

the step of using the error correction decoding technique to generate the block of decoded bits from the received signal comprises:

deinterleaving the received signal to generate a deinterleaved received signal

using the error correction decoding technique to generate the block of decoded bits from the deinterleaved received signal.

Paik et al. discloses, in an analogous art::

the step of using the error correction decoding technique(Fig 1, no. 44) to generate the block of decoded bits from the received signal (Fig 1. RX Data) comprises:

deinterleaving the received signal (Fig 1, received signal shown as input to block 42) to generate a deinterleaved received signal (Fig 1, shown as output of block 42)

using the error correction decoding technique(Fig 1, no. 44) to generate the block of decoded bits (Fig 1. RX Data) from the deinterleaved received signal (Fig 1. output of no. 42).

Wicker, in an analogous art, discloses that the use of a deinterleaver with error correction techniques as a way of reducing the effect of burst errors (page 424-426, section 16.1.).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify ABE et al. such that the received signal is first deinterleaved and then decoded by a error correction decoding technique as shown by Paik et al. in figure 1.

The motivation for adding an interleaver before the error correction decoder would be to reduce the effect of burst errors on the received signal. (Wicker, page 424-426, section 16.1.).

Claim 12

8. Claim 12 (dependent on claim 10) is rejected under 35 U.S.C. 103(a) as being unpatentable over the best mode of Abe et al. (EPO 0,600,095 A1).

Abe et al discloses all of the elements recited by claim10. (see rejection of claim 10 under 35 USC 102(b))

Abe et al does not explicitly disclose logic that sets the bit error rate estimate equal to the value that is based on the previously calculated bit error rate comprises: logic that sets the bit error rate estimate equal to a value that is equal to the previously calculated bit error rate comprises setting the bit error rate estimate equal to a value that is equal to a previously calculated bit error rate.

Abe et al Teaches in Column 3, lines 40-47 that the calculated BER is not accurate when an error occurs during decoding.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify Abe et al. such that it contains logic to disable updating the BER register that receives the calculated BER when an error occurs during decoding. (or equivalently, setting the bit error rate estimate equal to a value that is equal to the previously calculated bit error rate.) The effect of doing this would cause the previously calculated BER to be used as the current BER.

The motivation for making this modification would be to prevent updating the BER with an inaccurate BER calculation when an error occurs during decoding. (Column 3, lines 40-47)

Claim 13

9. Claim 13 (dependent on claim 10) is rejected under 35 U.S.C. 103(a) as being unpatentable over Abe et al. (EPO 0,600,095 A1)

Abe et al discloses all of the elements recited by claim10. (see rejection of claim 10 under 35 USC 102(b))

Abe et al does not explicitly disclose the logic that sets the bit error rate estimate equal to the value that is based on the previously calculated bit error rate comprises logic that sets the bit error rate estimate equal to a value that is predicted from one or more previously calculated bit error rates.

Abe et al Teaches in Column 3, lines 40-47 that the calculated BER is not accurate when an error occurs during decoding.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify Abe et al. such that it includes logic for averaging previously calculated BER in order to calculate a preset value for assignment as an estimated BER in the case where a decoder error has occurred.

The motivation for making this modification would be to prevent updating the BER with an inaccurate BER calculation when an error occurs during decoding. (Column 3, lines 40-47)

Claim 16

10. Claim 16 (dependent on claim 10) is rejected under 35 U.S.C. 103(a) as being unpatentable over ABE et al.(EPO 0,600,095 A1).

Abe et al. discloses all of the elements recited by claim 10. (see rejection of claim 10 under 35 USC 102(b))

Abe et al. does not disclose:

logic that uses the error correction decoding technique to generate the block of decoded bits from the received signal comprises:

a deinterleaver that deinterleaves the received signal to generate a deinterleaved received signal; and

logic that uses the error correction decoding technique to generate the block of decoded bits from the deinterleaved received signal.

Wicker, in an analogous art, discloses that the use of a deinterleaver with error correction techniques as a way of reducing the effect of burst errors (page 424-426, section 16.1.).

Paik et al. discloses, in an analogous art:

logic that uses the error correction decoding technique(fig.1, no. 44) to generate the block of decoded bits from the received signal (fig 1. RX Data) comprises:

a deinterleaver (Fig 1, 42) that deinterleaves (Fig 1, output of 42) the received signal (Fig 1. RX Data) to generate a deinterleaved received signal (Fig 1, output of 42); and

logic that uses the error correction decoding technique (Fig 1, no, 44) to generate the block of decoded bits from the deinterleaved received signal(Fig 1. output of 42).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify ABE et al. such that the received signal is first deinterleaved and then decoded by a error correction decoding technique as shown by Paik et al. in figure 1.

The motivation for adding an interleaver before the error correction decoder would be to reduce the effect of burst errors on the received signal. (Wicker, page 424-426, section 16.1.).

Allowable Subject Matter

Claims 8, 9, 17, & 18

11. Claim 8, 9,17, & 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The closest related art is ABE et al.(EPO 0,600,095 A1).

Abe et el. discloses the step of setting the bit error rate estimate equal to the value that is a preset bit error rate.

Abe et el. does not explicitly disclose the detailed steps of: selecting a value for the preset bit error rate. Specifically Setting the bit error rate estimate equal to a predetermined value that is not based on the previously calculated bit error rate if the block of decoded bits is at least an nth consecutively received block of decoded bits having at least one decoded bit that has an erroneous value, wherein n is a number greater than one; and otherwise setting the bit error rate estimate equal to the value that is based on the previously calculated bit error rate if at least one of the decoded bits from the block of decoded bits has an erroneous value.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to William Patrick Moore whose telephone number is (703)305-9727. The examiner can normally be reached on 8:30 - 5 PM If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on

(703)305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 746-7240.

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

William Patrick Moore

December 13, 2002

WM